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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,212	05/18/2001	Kozo Nakamura	82821	6761

7590 01/14/2004

Welsh & Katz
22nd Floor
120 South Riverside Plaza
Chicago, IL 60606-3913

EXAMINER	
SONG, MATTHEW J	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

AS

Office Action Summary	Application No.	Applicant(s)	
	09/856,212	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7 and 9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,7 and 9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 2 recites, "the step of adjusting said condition (a) and (b) by **narrowing** a distance between a heat shielding element equipped in a Czochralski method-based silicon single crystal" in lines 9-11. There is no support in the instant specification for "narrowing". The instant specification merely teaches, "changing a distance" on page 9 and "adjusting a distance" on page 10. The instant specification does not explicitly teach "narrowing".

3. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 3 recites, " the step of adjusting said conditions (a) and (b) by **decreasing** the pulling speed of the silicon single crystal" in lines 9-10. The instant specification does not explicitly teach

"decreasing" the pulling speed. The instant specification merely teaches "changing" the pulling speed on page 9.

4. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 7 recites, "a distance between the heat shielding element and the silicon melt becomes **narrower** along with pulling of the silicon single crystal ingot" in lines 6-8. There is no support in the instant specification for "narrower". The instant specification merely teaches, "changing a distance" on page 9 and "adjusting a distance" on page 10. The instant specification does not explicitly teach "narrowing".

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Shimanuki et al (JP 09-315882), where US 5,900,059 is used as an accurate translation and an accurate English translation can be provided upon request.

Shimanuki et al discloses a closed container **1**, a crucible element **18** which stores a melt, rotates and is vertically driven, a pulling element **21** for pulling an ingot, while rotating from said melt, a heating element **16** and a heat shielding element **4,5,6** and a drive mechanism **8** for moving the shielding element (Figs 1 and 4-7, '059 col 1, ln 15-50 and col 5, ln 10-55). Shimanuki et al discloses narrowing the distance between the heat shield and the melt in Fig 6, note the arrows indicating the downward direction of the heat shield.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264).

Iida et al teaches a single crystal ingot of silicon was pulled while varying the average pulling rate over a range of 1.0 mm/min and 0.4 mm/min. Iida et al also teaches the temperature gradient in an in-crystal descending temperature zone between a melting point of silicon and 1400°C in the vicinity of the solid-liquid interface was set as follows: G_e=45.0°C/cm and G_c=42.0 °C/cm, where G_e reads on applicant's G outer and G_c reads on applicant's G center. The ratio of G_e/G_c can be determined to 1.07 and at a pulling rate of 0.72 mm/min the V/G at the center is 0.16 mm^2/°C*min and at the outer periphery is 0.17 mm^2/°C*min (col 14, ln 20-67).

Iida does not teach temperature gradient in a pulling axis direction within a temperature range from silicon melting point to 1350°C. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida by attempting to optimize the temperature range by conducting routine experimentation.

Referring to claim 3, Iida et al is silent to the step of adjusting conditions (a) and (b) by decreasing the pulling speed of the silicon single crystal ingot. The pulling rate, V, is well known in the art to affect the V/G ratio. Also, changing the pulling rate will inherently change the temperature gradient in the single crystal, as evidenced by Morioka et al (US 4,783,235) below. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida et al by decreasing the pulling rate to obtain the processing condition taught by Iida.

Referring to claim 4, Iida et al is silent to a silicon wafer with decreased grown-in defects, this reads on applicant's relatively defect free, which is obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

Referring to claim 5, Iida et al is silent to a silicon perfect single crystal wafer free from grown-in defects obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

9. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hourai et al (US 5,954,873).

Hourai et al teaches the relationship of V/G and the position in the radial direction of the crystal in Fig 2, where V is the single crystal pulling rate (mm/min) and the inside-crystal temperature gradient in the direction of the pulling axis in a high temperature zone from the melting point of silicon to 1300°C. Hourai et al also teaches the single crystal pulling rate and the inside-crystal temperature gradient in the axial direction are two critical parameters for controlling the diameter of an oxidation-induced stacking fault (OSF) ring and the diameter of the OSF ring can be determined by the ratio of V/G (col 4, ln 50-60). Hourai discloses to compensate for changes in the temperature gradient of the crystal; the pulling rate is adjusted so that a constant V/G may be achieved (col 6, ln 55-60)

Hourai does not teach the parameter of a V/G=0.16-0.18 $mm^2/°C*min$ or a G outer/G center ≤ 1.10. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai by deriving the condition of claim 1, based on the profile of Fig 2.

Hourai does not teach temperature gradient in a pulling axis direction within a temperature range from silicon melting point to 1350°C. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai by attempting to optimize the temperature range by conducting routine experimentation.

Referring claim 3, Hourai discloses to compensate for changes in the temperature gradient of the crystal, the pulling rate is adjusted so that a constant V/G may be achieved (col 6, ln 55-60). Hourai et al does not teach decreasing the pulling rate. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai et al by

decreasing the pulling rate to obtain the desired V/G because the pulling rate is a result effect variable.

Referring to claim 4, Hourai et al is silent to a silicon wafer with decreased grown-in defects, which is obtained from the silicon ingot of claim 1. It is inherent to Hourai's invention to produce a silicon wafer with decreased grown-in defects because Hourai teaches similar growth conditions of a silicon single crystal ingot as applicant.

Referring to claim 5, Hourai et al is silent to a silicon perfect single crystal wafer free from grown-in defects obtained from the silicon ingot of claim 1. It is inherent to Hourai's invention to produce a silicon wafer with decreased grown-in defects because Hourai teaches similar growth conditions of a silicon single crystal ingot as applicant.

10. Claim 2 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264) or Hourai et al (US 5,954,873) in view of Shimanuki et al (JP 09-315882), where US 5,900,059 is used as an accurate translation and an accurate English Translation can be provided upon request.

Iida et al or Hourai et al teaches all of the limitations of claim 2, except the conditions (a) and (b) of claim 1 are adjusted by narrowing a distance between a heat shielding element equipped in a Czochralski method-based silicon single crystal production device and silicon melt along with pulling of the silicon crystal ingot.

In a method of growing a single crystal, note entire reference, Shimanuki et al teaches the heat history of a single crystal can be easily controlled by a shield cylinder, where the shield cylinder is designed to surround the semiconductor single crystal being lifted and is able to move

upward and downward to control the heat history (‘ 059 col 2, ln 15-67). Shimanuki et al also teaches by moving the shield cylinder it is possible to reduce the temperature gradient of the single crystal, which reduces as-grown defects (col 3, ln 15-25). Shimanuki et al also teaches lowering the shield cylinder during pulling (Fig 6 and ‘059 col 5, ln 10-55). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida et al or Hourai et al by using the movable heat shielding of Shimanuki et al to control the temperature gradients in a single crystal to obtain the processing conditions taught by Iida et al or Hourai et al and to reduce as-grown defects.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 5,942,032) in view of Luter (5,922,127).

Kim et al teaches a heat shield assembly for use in a crystal puller of the type used to grow monocrystalline silicon ingots according to the Czochralski method. Kim et al also teaches a crystal puller (12) includes a shell for isolating an interior, which includes a lower crystal growth chamber, this reads on applicant’s limitation of a closed container. Kim et al discloses a quartz crucible containing a molten semiconductor source, where the crucible is mounted on a turntable for rotation about a vertical axis and is capable of being raised with the growth chamber. Kim et al also discloses heating panels (24) heat the crucible (col 4, 42-67). Kim et al also teaches the heat shield assembly an intermediate heat shield (40), a lower heat shield (42) and an upper heat shield (36) (col 5, ln 15-65) and the heat shield assembly can be raised and lowered using the existing pulling mechanism of the crystal puller (12) (col 3, ln 15-20). Kim et al discloses the upper heat shield is positioned so that the portions of the ingot entering the upper

heat shield are approximately at 1150°C and inside the upper heat shield, heat transfer from the ingot to the sidewalls is reduced so that the instantaneous axial temperature gradient G_o is lessened in the portion of the upper heat shield (col 9, ln 40-50 and ln 25-27). Kim et al also discloses the lower heat shield prevents heat from radiating from the sidewalls of the crucible to the ingot (col 9, ln 15-22). Kim et al also discloses using the heat assembly (10) a high v/G_o ratio is achieved and the ratio of v/G_o is increased without changing the pull rate v, however variation in the pull rate may be employed to increase the v/G_o ratio (col 9, ln 55-67 and col 10, ln 1-10). Kim et al also discloses a winch, this reads on applicant's drive mechanism, is activated to move the heat shield assembly **10** and a switch is proved in the growth chamber to shut off the winch when the heat shield assembly is fully raised (col 8, ln 1-67)

Kim et al does not teach a pulling element for pulling a silicon single crystal ingot, while rotating.

In a method of pulling a monocrystalline ingot used to manufacture semiconductor wafers, Luter et al discloses a pulling mechanism (30) rotates a seed crystal C and moves it up and down through the growth chamber (col 4, ln 5-10). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim with Luter because counter-rotating the crystal and crucible prevents the exchange of impurities between the melt directly below the crystal and the residual melt, note Chapter 2.5 of Zulehuler and Huber.

The combination of Kim et al and Luter et al is silent to narrowing the distance of the heat shielding element and silicon melt. The limitation is viewed by the Examiner as the intended use of the claimed apparatus. The combination of Kim et al and Luter et al teach the heat shield

assembly can be raised and lowered using the existing pulling mechanism of the crystal puller (12) (Kim col 3, ln 15-20); therefore would be capable of performing the claimed intended use.

Referring to claim 7, the combination of Kim and Luter teach a heat shield assembly **10**, which controls the temperature gradient in a pulling axis direction, this reads on applicant's control means and a winch (col 8, ln 5), this reads on applicant's drive mechanism and switch, which instructs the drive mechanism to stop.

12. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi et al. (US 5,931,662) in view of Iida et al (US 5,968,264).

Adachi et al teaches the preferred annealing conditions for forming defect-free region, where defect-free reads on applicant's perfect crystal, is to ramp up to a temperature in excess of 1100°C and annealing preformed at temperatures ranging from 500°C to 900°C for more than 10 minutes can provide IG functions by forming oxide precipitates, BMD. Adachi et al also teaches BMD for IG functions can also be formed by ramping up from 500°C to 900°C at a rate of 0.5°C/min (col 10, ln 60-67). Adachi et al discloses maintaining a temperature between 500°C to 900°C for more than 10 minutes during the ramp down process following sustained heating at a temperature in excess of 1100°C makes it possible to provide IG functions by forming BMD at a rate of 0.5°C/min (col 11, ln 5-15). Adachi et al also discloses silicon single crystal wafers were loaded into an annealing boat and into a furnace pre-heated to 700°C (col 11, ln 50-60). Adachi teaches in Fig 11 and 12 indicating the relationship between surface depth and oxygen concentration and the results indicate DZ layers had been secured in all wafers after annealing (col 12, ln 46-55)

Adachi et al does not teach the single crystal wafer is relatively defect free.

In a method of forming a single crystal wafer, Iida et al teaches a method of forming a single crystal wafer with very few crystal defects, this reads on applicant's relatively defect free wafer, and when this wafer undergoes an oxygen precipitation heat treatment and is observed by means of X rays, uniform precipitation contrast is observed over the surface thereof and a small number of striation rings is observed (col 13, ln50 to col 14, ln 15). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi et al with Iida et al's silicon wafer to form a uniform precipitation.

The combination of Adachi et al and Iida et al does not teach a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment is 500°C or less. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi by attempting to optimize same by conducting routine experimentation.

Referring to claim 10, the combination of Adachi et al and Iida et al is silent to a uniform distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment. It is inherent to the combination of Adachi et al and Iida et al's invention to uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment because the combination of Adachi et al and Iida et al teaches a similar heat treatment with an ultimate temperature set in a range of 500-900°C at a similar ramping rate of 0.5 °C/min as applicant.

Referring to claim 11, the combination of Adachi et al and Iida et al is silent to adjusting the distribution of an oxide precipitate density of the silicon single crystal wafer after the heat

treatment. It is inherent to the combination of Adachi et al and Iida et al's invention to uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment because the combination of Adachi et al and Iida et al teaches a similar heat treatment with an ultimate temperature set in a range of 700-900°C as applicant.

Referring to claim 12, Adachi teaches the oxygen concentration is less than $13x10^{17}$ atoms/cm^3 in the DZ layer in Figs 11 and 12. If Adachi does not teach this in Figs 11 and 12, then it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi by attempting to optimize same by conducting routine experimentation.

Referring to claim 13, the combination of Adachi et al and Iida et al teaches silicon wafers were annealed under similar conditions as taught by applicant.

Response to Arguments

13. Applicant's arguments with respect to claims 2-5 and 7 have been considered but are moot in view of the new ground(s) of rejection.

14. Applicant's arguments filed 10/10/2003 have been fully considered but they are not persuasive.

Applicant's arguments against Hourai et al are noted but are not found persuasive. Applicant alleges that Hourai et al only describes changing the pulling speed of the ingot and does not describe that the pulling speed of the ingot might be decreased in conjunction with the pulling of the ingot. Hourai et al teaches a V/G ratio is controlled and V is the pulling rate.

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai et al to obtain the desired V/G by decreasing the pulling speed to change the V/G ratio because V is known to affect the V/G ratio. It is unclear to the Examiner how a pulling speed is not changed in conjunction with the pulling of the ingot, as alleged by applicant, because the pulling speed of the ingot occurs during pulling of the ingot. Applicant's also alleges that the invention is not a mere optimization of the techniques of Hourai et al. There is no showing of an unexpected result; therefore this argument is not found persuasive, note MPEP 2144.05. The V/G ratio is show by Hourai et al to be a result effective variable; therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai et al by optimizing the condition to obtain same by conducting routine experimentation.

In response to applicant's argument that the combination of Kim and Luter does not teach a drive mechanism for moving a heat shielding element so that a distance between the heat shielding element and the silicon melt becomes narrower along with pulling of the silicon single crystal ingot, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). The combination of Kim et al and Luter et al teach the heat shield assembly can be raised and lowered using the

existing pulling mechanism of the crystal puller (12) (Kim col 3, ln 15-20); therefore would be capable of performing the claimed intended use.

Applicant's arguments against the combination of Adachi et al and Iida et al are noted but are not found persuasive. Applicant alleges that the heat treatment of Adachi et al is a high temperature heat treatment. Adachi et al teaches BMD for IG functions can be formed by ramping up from 500°-900°C at a rate of between 0.5°C/min and 5°C/min and annealing conditions for forming a defect-free region is to ramp up to a temperature in excess of 1100°C (col 10, ln 60-67). The difference between instant invention and Adachi et al is the ultimate temperature. Adachi et al teaches annealing from 500-900°C for forming BMD for IG functions and further annealing at a temperature greater than 1100°C to from a defect-free region. Therefore, the annealing from 500-900°C for forming BMD for IG functions of Adachi et al reads on applicant's heat treatment set in a range of 700-900°C and the instant invention merely eliminates the subsequent heating of Adachi et al. Elimination of a step and its function is held to be obvious (MPEP 2144.04).

In response to applicant's argument that the treatment target of the present invention and Adachi et al are different, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Adachi

et al teaches similar temperatures and ramping rates; therefore would be capable of performing the intended use.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Von Ammon et al ("The dependence of bulk defects on the axial temperature gradient of silicon crystal during Czochralski growth") teaches the critical pulling rate varies with the crystal diameter and the type of heat shield (abstract).

Bischoff et al (US 4,437,922) teaches heating a silicon wafer from 450°C to an ultimate temperature of 800°C at a rate 0.84°/min (Fig 2 and claim 8).

Morioka et al (US 4,783,235) teaches to reduce the temperature gradient, the pulling speed should be small in a LEC process for forming single crystals (Abstract and col 10, ln 1-5).

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Matthew J Song
Examiner
Art Unit 1765

MJS

NADINE G. NORTON
PRIMARY EXAMINER